1 Introduction

Despite the many comprehensive references on photovoltaic design, there still exists a wide expanse separating theory from practice. It is therefore an important educational experience for students to work through the process of solar cell fabrication under controlled conditions. Although this requires a sophisticated technological infrastructure, we are fortunate enough here at the University of Utah to possess access to a modern fabrication facility. This provides students with a fantastic opportunity for a “hands on” approach to photovoltaic systems as a supplement to their classroom education.

The goal of this report is to provide a procedural tutorial on the manufacture of solar cells through the resources provided by the University of Utah NanoFab. For each characterization step, an example data set will be provided out of our own measurements to help illustrate the expected nature of the results. Although we attempt to explain as much as possible where we can, it is important to emphasize that the reader is ultimately responsible for proper training on the use of equipment by the NanoFab staff. Many steps in this procedure also require the use of dangerous chemicals and equipment, so students and TAs should be especially confident in their ability to follow proper safety rules before engaging in this procedure.

Finally, it is important to remember that this process is by no means set in stone. Rather, this document simply represents the final product of a long series of process iterations that finally resulted in a reliable photovoltaic device. Many steps in the procedure are difficult to engineer from a solid theoretical perspective, while others are simply precautionary in nature and may not even be necessary. Students and TAs should therefore feel free to attempt future modifications with this procedure in order to secure higher efficiencies. Readers are especially encouraged to keep proper lab notebooks and document their progress as they attempt to follow this tutorial and present any significant results for future generations of students.

For further reading on fabrication processes, we highly recommend *Semiconductor Devices: Physics and Technology*, by S. M. Sze [1]. We shall be borrowing heavily from this text throughout this report. It is also assumed that the reader has been properly trained in the use of any NanoFab resources required by this procedure.
Table 1: Siltronix wafer specifications.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Prime - Czochralski</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diameter</td>
<td>2.0 inches</td>
</tr>
<tr>
<td>Type &amp; Dope</td>
<td>P-Boron</td>
</tr>
<tr>
<td>Orientation</td>
<td>(100) ± 5°</td>
</tr>
<tr>
<td>Resistivity</td>
<td>1–10 Ω·cm</td>
</tr>
<tr>
<td>Thickness</td>
<td>350 μm ± 25 μm</td>
</tr>
<tr>
<td>Surface</td>
<td>Double Sided Polish</td>
</tr>
</tbody>
</table>

Table 2: Wafer thickness measurements with the Allied High-Tech Dial Indicator.

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Thickness (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1)</td>
<td>326</td>
</tr>
<tr>
<td>(2)</td>
<td>338</td>
</tr>
<tr>
<td>(3)</td>
<td>340</td>
</tr>
<tr>
<td>(4)</td>
<td>337</td>
</tr>
<tr>
<td>(5)</td>
<td>343</td>
</tr>
<tr>
<td>Mean</td>
<td>337</td>
</tr>
</tbody>
</table>

2 Wafer Characterization

The first step in our lab procedure is to acquire silicon wafers. For this tutorial we shall be working with prime-grade wafers manufactured by Siltronix [2]. The wafer specifications may be found in the commercial documentation and the relevant details are summarized in Table 1. Once our wafers are in hand, we can then verify some of the key design parameters by using the test instruments of the NanoFab.

The first measurement to perform is a verification of thickness using the Allied High-Tech Dial Indicator (basically a sophisticated caliper). Although wafer specifications are given at 350 μm ± 25 μm, an exact measurement is necessary in order to produce an accurate calculation of resistivity. There will also tend to be some variation on the order of ± 10 μm within the same wafer, so it is instructive for students to observe this firsthand. The procedure is therefore to take five measurements of thickness and then use the mean value for all future calculations. An example data set is summarized in Table 2.

The next step is to perform a resistivity test by using the four-point probe method. For a small constant current $I$ and voltage measurement $V$, the sheet resistivity of a material is determined by the expression

$$\rho_s = \frac{\pi}{\ln 2} \frac{V}{I}.$$  \hspace{1cm} (1)

Note that the factor of $\pi/\ln 2$ is approximately 4.53. Consequently, it is common for four-point probe devices to produce scaled currents around this value (i.e.; 453 μA, 4.53 mA, 45.3 mA, etc). This causes the output voltage reading to produce a direct measurement in units of Ω/□. For example, a typical voltage reading from our wafers may produce a value of $V = 160$ mV under a current excitation of $I = 4.53$ mA. The sheet resistivity would therefore be $\rho_s = 160$ Ω/□.
With sheet resistivity in hand, we may now calculate the physical resistivity of our wafers using the expression

$$\rho = \rho_s t,$$

where \( t \) is the mean thickness of the wafer. Using Table 2, we may use \( t = 337 \, \mu\text{m} \) to find \( \rho = 5.4 \, \Omega \cdot \text{cm} \). Comparing this result with the product specifications, we find that is well within the expected range of values.

The final step in this segment is to calculate the impurity doping concentration of our wafers. Looking again to Table 1, we find that our wafers are doped with boron. Since boron is a donor impurity in silicon, our wafers are p-type semiconductors. The relationship between resistivity and donor concentration is then found using the expression

$$\rho = \frac{1}{q \mu_p N_A},$$

where \( q = 1.602 \times 10^{-19} \, \text{C} \) is the electron charge, \( \mu_p \) is the hole mobility in silicon, and \( N_A \) is the hole concentration. The hole mobility is not exactly a constant value in silicon, but actually tends to vary as a function of \( N_A \) according to the relation

$$\mu_p(N_A) = 48 + \frac{447}{1 + \left( \frac{N_A}{6.3 \times 10^{16}} \right)^{0.76}},$$

where \( \mu_p \) has units of \( \text{cm}^2/\text{V} \cdot \text{s} \). Figure 1 shows a plot of \( \rho \) versus \( N_A \), which tells us that a resistivity of \( 5.4 \, \Omega \cdot \text{cm} \) corresponds to an impurity concentration of roughly \( N_D \approx 2 \times 10^{15} \, \text{cm}^{-3} \). This value will prove useful later on when we attempt to determine junction depth after n-type doping.

## 3 Oxide Growth

Now that our wafers have been characterized, the next step is to grow a thin layer of oxide around the edges. This layer will serve as a protective barrier during the phosphorus diffusion process as well as act as an insulator between the top and bottom contacts of the cell. The exact thickness of the barrier itself is not very important, just so long as the oxide is deep enough to serve these ends. We shall therefore specify a target thickness of 0.5 \( \mu\text{m} \) for the oxide as illustrated in Figure 2.

Two types of chemical reaction may be utilized to grow oxide on silicon. The first is called dry oxidation and is governed by the reaction

$$\text{Si (solid)} + \text{O}_2 \, (\text{gas}) \rightarrow \text{SiO}_2 \, (\text{solid}).$$

Another useful reaction is called wet oxidation because it occurs in the presence of water vapor. The governing reaction is therefore

$$\text{Si (solid)} + 2\text{H}_2\text{O} \, (\text{gas}) \rightarrow \text{SiO}_2 \, (\text{solid}) + 2\text{H}_2 \, (\text{gas}).$$

The primary difference between these reactions is that wet oxidation tends to occur at a much faster rate than dry oxidation. It is also worth noting that these reactions can also occur even in ordinary air at room temperature. The result is a native oxide layer on all silicon wafers that slowly
Figure 1: Resistivity of crystalline silicon as a function of p-type impurity concentration. A resistivity value of $\rho = 5.4 \ \Omega \cdot \text{cm}$ corresponds to a doping concentration of $N_D \approx 2 \times 10^{15} \ \text{cm}^{-3}$.

Figure 2: Thermal oxidation on a silicon wafer. (a) The bare wafer of crystalline silicon (c-Si) before oxidation. (b) Wafer with a 500 nm layer of SiO$_2$ after thermal oxidation.
grows thicker over time. Fortunately, the rate of reaction at standard temperature and pressure is extremely slow. Even after several days, the thickness of a native oxide layer will generally saturate at no more than 1–2 nm [4].

Although the exact equations for oxide growth are intricate and complex, it is possible to simplify matters by approximating the oxide thickness as a linear function of time. The growth rate itself depends heavily on such factors as ambient temperature, gas flow, and even crystal orientation, but can still be reasonably approximated for our current needs. For example, the growth rate for dry oxidation at 1050 C generally ranges between 60–80 nm per hour. For wet oxidation, the rate increases can almost reach 500 nm per hour. Consequently, one hour of wet oxidation at 1050 C should be enough to produce the desired thickness for our application. It is also common to pad this value with 5 minutes of dry oxidation both before and after the hour of wet oxidation.

The instrument of choice for performing thermal oxidation in the NanoFab is the Diffusitron Mark IV furnace. This device is simply a pack of quartz tubes designed to bake wafers at very high temperatures. One tube is specifically set aside for thermal oxidation and is connected to a series of gas flow valves. While flowing oxygen through the tube, a standard flow rate that works well is 7.0 SLM (standard liters per minute) for both wet and dry oxidation.

Once the oxide growth is complete, we can verify the outcome in two ways. The first method is somewhat crude, and simply involves a visual inspection of the color of the wafer. For ≈ 500 nm of oxide growth, the color of the wafer should have changed from a shiny gray into a dark violet. Charts are also freely available online that give a full spectrum of colors over a wide range of oxide thicknesses. The second method is more precise, and utilizes direct optical inspection with the Nanospec 3000. After 5 minutes of dry oxidation, 60 minutes of wet oxidation, and another 5 minutes of dry again, most wafers will tend to grow between 450–480 nm of oxide. Due to turbulence of air flow within the furnace, it is also common for wafers on the edge of the quartz boat to exhibit perhaps 400–420 nm of oxide thickness. This can be partially alleviated through the use of sacrificial wafers at each end of the boat, thereby producing greater uniformity for the test wafers packed between. However, this step is strictly aesthetic since the exact thickness of oxide buffer is not a crucial design parameter.

4 Oxide Etching

The next step in our procedure is to etch an opening in the top side of the wafer for phosphorus to pass during diffusion. This is accomplished through the use of a process known as photolithography and requires the use of very dangerous chemicals. Students and TAs alike should therefore take great care to carefully follow safety guidelines during this step.

Photolithography can be a complex and tedious process, but is also very powerful at producing precise features in a semiconductor device. The procedure itself is graphically summarized in Figure 3 and expressly detailed below:

- Apply photoresist along the wafer using Shipley S1813 positive photoresist (PR). Using the Headway EC101, spin-coat at 2000 rpm for 45 seconds and then bake on a hotplate at 115 C for 60-90 seconds. Repeat for the opposite side of the wafer. Further information is available from the S1800 product brochures supplied by Shipley [5].

- Align a photomask over the top surface using the OAI 200. The specific photomask for this step is simply a sheet of aluminum with a small hole punched in it. The hole diameter was
Figure 3: Graphical illustration of the photolithography procedure. (a) Spin-coat top and bottom with photoresist. (b) Deposit photomask over top surface. (c) Expose to UV light. (d) Bathe in developer solution. (e) Bathe in HF solution. (f) Rinse with acetone.
specifically chosen to be slightly less than 2.0 inches so as to leave a ring of unexposed PR. This will serve as a barrier against accidental electrical contact between the top and bottom of the wafer via the edges. A plastic sheet of transparency paper serves well as an intermediate barrier to protect against scratches on the wafer.

- Expose the wafer under ultraviolet (UV) light for 14 seconds at 250 mW power output. Sections of the PR that are exposed to UV will be chemically altered while the rest will remain unchanged. When dipped into a special developer solution, only the exposed PR will dissolve.

- Rinse the wafer in AZ300 developer until exposed PR is fully dissolved. This usually takes between 30–60 seconds. Be careful not to over-develop the wafer.

- Dip the wafer in buffered oxide etch. The etch rate is listed at 90 nm per minute, so 6 minutes is more than enough time to guarantee full removal of the oxide layer. BEWARE: this step is especially dangerous due to the use of hydrofluoric acid. Always remember to exercise proper safety procedures. After etching, rinse in deionized water for 5 minutes to ensure total removal of acid from the wafers.

- Rinse wafers in solvent to remove excess photoresist. Acetone and isopropanol work well for this step.

After etching is completed, there should be a large crater of exposed silicon on the top side of the wafer and a ring of SiO\textsubscript{2} around the edges. If performed properly, the ring on top and the film on the bottom should have remained perfectly untouched by the acid. Proper etching can also be verified by remeasuring oxide thickness with the Nanospec.

5 Phosphorus Doping

With the top side of the wafer exposed, we can now dope it using phosphorus diffusion with the PhosPlus TP-470 planar dopant sources [6]. This step requires the phosphorus doping tube in the Diffusitron Mark IV furnace and is illustrated in Figure 4. The procedure works by heating up a wafer of P\textsubscript{2}O\textsubscript{5} to a temperature between 900–1200 °C. This causes the wafer to sublimate directly into the surrounding air, thus providing a rich source of phosphorus at high kinetic energy. If a silicon wafer is placed directly alongside the dopant source, atoms of phosphorus will accumulate along the surface and diffuse into the bulk silicon. Due to the oxygen content of the dopant source, a thin layer of oxide will also accumulate along the surface of the silicon. In practice, this layer tends to reach anywhere between 40–80 nm, and may therefore be removed by a quick 60 second bath in the buffered oxide etch.

The physical process of phosphorus doping can be simply modeled by applying the diffusion equation in one dimension. Letting \( C(x, t) \) represent the concentration of dopants in the silicon wafer as a function of depth \( x \) from the surface and time \( t \) in seconds, the 1D diffusion equation is written as

\[
\frac{\partial}{\partial t}C(x, t) = D \frac{\partial^2}{\partial x^2}C(x, t),
\]

where \( D \) is called the diffusion coefficient or diffusivity. If we pretend that the wafer is infinitely thick (which it practically is for this application), then we may assume a constant surface concentration \( C(0, t) = C_s \) and let \( C(\infty, t) = 0 \). Under these two boundary conditions, the solution is
Figure 4: Phosphorus doping illustrated. (a) Phosphorus atoms from the dopant source bombard the top surface of the exposed wafer. (b) A thin layer of n-type semiconductor is produced at the surface of the wafer. A thin oxide layer is also produced that needs to be removed.

The function \( \text{erfc}(x) \) is called the complementary error function, and is written as

\[
\text{erfc}(x) = \frac{2}{\sqrt{\pi}} \int_x^\infty e^{-t^2} \, dt .
\]

The two unknown parameters we need in order to generate a solution are \( C_s \) and \( D \). Unfortunately, both of these parameters are not easily obtained. The best we can do for now is to choose reasonable values based on physical arguments and remember that the reality of our process may potentially behave very differently. For example, the exact value for \( C_s \) is determined by such factors as the rate of sublimation from the PhosPlus wafers and the kinetic properties of deposition onto the adjacent silicon wafers. Although we have very little idea of how to realistically model such a process, we do know that there exists a solid-solubility limit between phosphorus and silicon. At 1050 °C, this value is approximately equal to \( 10^{21} \) atoms per cm\(^3\). Anything beyond this value and phosphorus is physically unable to form a diffusive solution inside of a crystalline silicon lattice. Because this is roughly 1/500th of the physical concentration of silicon atoms in a crystal, even a very inefficient transfer of phosphorus atoms to the silicon surface might easily push this limit. Consequently, it seems reasonable to assume a value of \( C_s = 10^{21} \) cm\(^{-3}\) as the surface concentration.

The diffusivity of phosphorus in silicon is an even more difficult problem because \( D \) is not a simple, constant value as one would hope. Rather it depends strongly on such factors as concentration and temperature. For low concentrations of phosphorus in silicon, the diffusivity as a function of temperature \( T \) (in Kelvins) can be expressed as [7]

\[
D(T) = 3.85 e^{-3.66eV/k_B T} \quad (\text{cm}^2/\text{s}) ,
\]

where \( k_B = 8.617 \times 10^{-5} \text{ eV/K} \) is Boltzmann’s constant. Inserting a temperature of 1050 °C therefore produces a value of \( D = 4.40 \times 10^{-18} \text{ cm}^2/\text{s} \). Figure 5(a) shows the calculated concentration profile for phosphorus diffusion into silicon after baking for 60 minutes at \( T = 1050 \) °C. The red line indicates the background concentration of boron dopants at \( 2 \times 10^{15} \text{ cm}^{-3} \). The crossover point between these two curves at nearly 0.8 µm represents the transition between n-type and p-type silicon.
silicon. Consequently, we see that the junction depth of our wafer depends strongly on the time and temperature of baking during phosphorus diffusion.

Although this analysis presents a nice theoretical picture of phosphorus diffusion, the reality of the situation is much more complex. At high phosphorus concentrations in crystalline silicon ($> 4 \times 10^{19}$ cm$^{-3}$), the diffusivity $D$ follows a much more complex profile. The net result is a nonlinear solution to the diffusion equation that is much more difficult to solve analytically. Figure 5(b) shows a set of more realistic profiles derived from empirical data [1]. For low values of surface concentration, it is clear that the profiles indeed follow the ideal behavior. However, for high surface concentrations, a “kink” will manifest in the profile that deviates from the idealized curve. If we had access to the proper measurement tools, it would be possible to verify this behavior for ourselves and tune the fabrication process accordingly. Unfortunately, since we do not possess such access, we can only rely on purely theoretical arguments for determining the concentration profile and subsequent junction depth. Between this analysis and the information provided in the product brochures [6], the best we can say is that the junction depth most likely lies somewhere between 1–3 $\mu$m underneath the silicon wafer surface.

Upon successful phosphorus doping, the next step is to perform another acid etch of the bottom surface. This may be accomplished by following the same photolithography procedure as outlined in Figure 3. However, once the back side is etched, the top and bottom of the wafer will be visually indistinguishable from each other. To help keep track of which end is up, it is recommended that another four-point probe measurement be performed on the top side of the wafer before etching. Bear in mind that because the wafer is no longer uniformly doped, the actual value itself will not be particularly meaningful. Fortunately, this is not a problem since the only goal for this step is to record a physical voltage that distinguishes the top side from the bottom. Figure 6 shows a diagram of the wafer before and after etching the bottom surface.
Aluminum Deposition

At this point, there should be smooth craters etched into both the top and bottom faces of the wafer. We are therefore ready to begin depositing aluminum contacts. The bottom face will have a solid contact that covers the entire area, while the top face will have a thin grid of metal contacts. This provides a uniform coverage for charge collection while simultaneously allowing light to enter the surface of the silicon. The contact pattern itself is printed on an

Figure 7 illustrates the procedure for aluminum deposition on the wafer. The details for this step are explained below.

- Following the same procedures as before, spin coat a layer of photoresist on the top and bottom faces of the wafer. Develop the bottom side of the wafer to expose another crater for etching.

- Etch the bottom surface for 5 minutes in buffered oxide etch to expose the bare silicon underneath. Again, remember to exercise proper safety rules when working with hydrofluoric acid.

- Develop the contact pattern on the top side of the wafer.

- Deposit aluminum on the bottom side of the wafer using the Denton Discovery 18. Flip the wafer over and deposit again on the top side. The deposition rate for aluminum on this machine is given by $0.3 \text{ nm/min} \cdot \text{W}$. However, because of the presence of photoresist in the chamber, it is recommended that power output be limited to 50 W. The deposition rate is therefore limited to 15 nm/min. The precise thickness of the aluminum contacts is not terribly important, just so long as it is thick enough to withstand scratches and form a decent contact. A value of 300 nm is reasonable for these goals, therefore giving a total deposition time of 20 minutes.

- Wash the wafer in an ultrasonic bath of acetone using the Fisher Scientific FS30H. This removes the photoresist and excess aluminum. Complete removal usually takes somewhere between 1–3 minutes.

Annealing

With the aluminum contacts now deposited, the wafer is almost a fully functional photovoltaic device. However, deposition of aluminum generally does not form an clean contact with silicon. We can rectify this problem by *annealing* the wafer in the Diffusitron furnace. The exact recommended
Figure 7: Aluminum deposition procedure. (a) Spin coat photoresist on both sides of the wafer and develop the bottom surface. (b) Etch oxide layer from the bottom. (c) Develop contact pattern on the top side. (d) Aluminum deposition on top and bottom. (e) Ultrasonic bath in acetone.
Figure 8: I-V curves for the solar cell immediately after aluminum deposition. (a) Before annealing, the poor Ohmic contacts manifest as a large series resistance. (b) After annealing, the diode response is much more ideal (note that current saturation on the instrument occurs at -100 mA).
Figure 9: Aluminum-silicon phase diagram.
The solution to the problem of junction spiking is to prevent silicon from diffusing into the aluminum contacts. One method is to use an aluminum target that comes already saturated with 1.0 % silicon. This prevents the silicon from diffusing into the contacts because the aluminum is already pressed beyond the solid solubility limit.

8 Analysis

Figure 11 shows the final J-V curves for an example wafer under calibrated AM 1.5 illumination using the silicon-aluminum target. One of the first problems immediately apparent is the odd “kink” behavior between -0.5 V and 0.0 V. It is currently unclear what exactly is causing this issue with our wafers, but it seems to be a form of saturation under a full sun of illumination. Since this will certainly perturb our final efficiency calculations, it is helpful to attenuate the incident light by applying a half-power filter to the incident spectrum from our AM 1.5 source. This produces the half-sun curve shown in red and exhibits a much more well-behaved response.

Figure 10: Junction spiking between an aluminum-silicon contact. (a) Graphical depiction. (b) I-V response curve. Junction spikes manifest as a large shunt resistance under reverse bias.

The first parameter of interest is the fill factor, defined as

$$FF = \frac{I_mV_m}{I_{sc}V_{oc}},$$  \hspace{1cm} (11)

where $I_m$ and $V_m$ are the current and voltage at the max-power point in the curve, $I_{sc}$ is the short-circuit current, and $V_{oc}$ is the open-circuit voltage. Performing this calculation on the half-sun data reveals a net fill factor of $FF = 0.425$. If we now define $S_i = 1.0 \text{ kW/m}^2$ as the incident solar power density, efficiency may be calculated using

$$\eta = \frac{I_{sc}V_{oc}FF}{AS_i},$$  \hspace{1cm} (12)

where $A = 20.3 \text{ cm}^2$ is the area of the wafer. Using $I_{sc} = 6.7 \text{ mA}$, $V_{oc} = 0.52 \text{ V}$, and $S_i = 500 \text{ W/m}^2$ finally gives us a net efficiency of 1.45 %. However, due to the 0.5 cm ring of oxide around the edges of the wafer, the true area of active material is more accurately $A = 13.1 \text{ cm}^2$. This correction produces an efficiency value of $\eta = 2.26 \%$. 
Figure 11: J-V curves for the final cell under calibrated illumination by an AM 1.5 source.

Two other parameters of interest are the series and shunt resistances, $R_s$ and $R_{sh}$. These can be measured by noting that $R_s$ tends to dominate the J-V characteristics under forward bias while $R_{sh}$ dominates under reverse. One simple method for estimating $R_s$ is to compute $-dV/dI$ near the open-circuit voltage point (the plotted data automatically carries a negative sign by convention in order to flip the curves upside down). Performing this calculation on the half-sun data yields

$$R_s = \frac{dV}{dI} \bigg|_{V=V_{oc}} = 3.35 \ \Omega . \quad (13)$$

Similarly, $R_{sh}$ may be estimated by simply calculating $dV/dI$ while under significant reverse bias.

$$R_{sh} = \frac{dV}{dI} \bigg|_{V=-2 \ \text{V}} = 834 \ \Omega . \quad (14)$$

9 Conclusions and Future Changes

The procedure outlined in this paper has proved itself to be successful at generating reliable results for a group of 12–14 students. Using the University of Utah NanoFab facility, our wafers consistently produced rectifying junctions that exhibited a detectable photovoltaic effect. However, analysis also indicates that efficiencies are limited to perhaps 2–3 % at most. One likely culprit for our low efficiency is sodium contamination [8]. Students should therefore study this problem in detail and find ways to remove it from the procedure in subsequent iterations.

Another avenue for efficiency gain involves the 0.5 cm ring of oxide around top side of our wafers, reducing the active collecting area of the cell by 35 %. In principle, this ring is intended to
eliminate any potential risk for electrical shorts that might develop between the top and bottom surfaces. However, it is unknown how much of a risk this actually is, and future students are encouraged to investigate the necessity of this feature.

Although we currently have photomasks available for deposition of the top-layer contacts, the overhead transparencies on which they are printed may not last forever. Students should therefore be encouraged to devise their own photomask layers for future implementations. It would also be useful for future TAs to put together a tutorial on this processes so that everyone can take part in the process more readily.

Further changes to the procedure involve the exact parameters used for such actions as spin coating and annealing. Although the current parameters seem to work well enough, there is a great deal of apparently arbitrary values littered throughout the procedure. For example, the oxide thickness of 500 nm is chosen as a seemingly decent value for protecting the wafer against phosphorus diffusion, but little information exists on phosphorus penetration through SiO2. The exact parameters for annealing are also somewhat arbitrary and seem to vary between processes across different educational facilities around the nation. Students are therefore encouraged to investigate the underlying physics of such steps in greater detail and perhaps refine the specific parameters for greater reliability and efficiency in the future.

References


